## **ABSTRACT**

Aspects for increased noise immunity for clocking signals in high speed digital systems are described. The aspects include buffering a differential clock signal with a single buffer circuit for a plurality of load circuits and configuring the single buffer circuit to adjust to alterations in the number of load circuits receiving the differential clock signal. The configuring achieves a constant bandwidth and voltage level for the clock signal output while adjusting to alterations in the number of load circuits.

5